AMENDMENTS TO CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A logic data analyzer for a test sample, comprising:

a control circuit adapted for reading test data from said test sample;

a memory, having a predetermined memory space, controlled by said control circuit to store said test data;

a compressor electrically coupled between said control circuit and said memory to compress said test data for reducing a size thereof before storing in said memory, such that said compressed test data is stored in said memory space of said memory to maximize said memory space of said memory to be utilized for storing a complete series of said test data of said test sample; and

a transmission interface electrically connected to said control circuit for connecting to a computer having a display means, wherein when said memory space of said memory is used up, said control circuit fetches said test data in said memory for directly transmitting said fetched test data to said computer through said transmission interface so as to display said fetched test data on said display means.

2. (Previously Presented) The logic data analyzer as recited in claim 1, wherein said control circuit controls said compressor for decompressing said fetched test data before transmitting said fetched test data to said computer.

3. (Previously Presented) The logic data analyzer as recited in claim 1, wherein said control circuit reads said test data in digital form from said test sample which embodies a digital circuit.

4. (Previously Presented) The logic data analyzer as recited in claim 2, wherein said control circuit reads said test data in digital form from said test sample which embodies a digital circuit.

5. (Previously Presented) The logic data analyzer as recited in claim 3, wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time interval.

6. (Previously Presented) The logic data analyzer as recited in claim 4, wherein control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time interval.

7. (Previously Presented) A logic data analyzer for a test sample, comprising:

a control circuit adapted for reading test data from said test sample;

a memory, having a predetermined memory space, controlled by said control circuit to store said test data;

a compressor electrically coupled between said control circuit and said memory to compress said test data for reducing a size thereof before storing in said memory, such that said compressed test data is stored in said memory space of said memory to maximize said memory space of said memory to be utilized for storing a complete series of said test data of said test sample; and

a display means electrically coupled to said compressor, wherein when said memory space of said memory is used up, said control circuit fetches said test data in said memory to display said fetched test data on said display panel.

8. (Currently Amended) the logic data analyzer as recited in claim 7, wherein said control circuit controls ~~said~~ a decompressor for decompressing said fetched test data before displaying said fetched test data on said display means.

9. (Previously Presented) The logic data analyzer as recited in claim 7, wherein said control circuit reads said test data in digital form from said test sample which embodies a digital circuit.

10. (Previously Presented) The logic data analyzer as recited in claim 8, wherein said control circuit reads said test data in digital form from said test sample which embodies a digital circuit.

11. (Previously Presented) The logic data analyzer as recited in claim 9, wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time interval.

12. (Previously Presented) The logic data analyzer as recited in claim 10, wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time interval.

13. (Currently Amended) A method of processing test data from a test sample to a logic data analyzer which comprises a control circuit, a memory, and a compressor, comprising the steps of:

(a) reading said test data from said test sample to said control circuit;

(b) compressing said test data by said compressor to reduce a size of said test data;

(c) storing said compressed test data in said memory to maximize a memory space of said memory to be utilized for storing a complete series of said test data of said test sample; and

(d) displaying said test data on a display ~~means~~ panel which is electrically coupled with said compressor, wherein when said memory space of said memory is used up, said control circuit fetches said test data in said memory to ~~disp0lay~~ display said fetched test data on said display panel.

14. (Currently Amended) The method as recited in claim 13, wherein said control circuit ~~si~~ is electrically connected to a computer via a transmission interface to transmit said test data to said

computer so as to display said test data on said display means built-in with said computer when said memory space of said memory is used up.

15. (Previously Presented) The method as recited in claim 13, after the step (c), further comprising a step of decompressing said fetched test data before displaying said fetched test data on said display panel.

16. (Previously Presented) The method as recited in claim 14, after the step (c), further comprising a step of decompressing said fetched test data before displaying said fetched test data on said display panel.

17. (Previously Presented) The method as recited in claim 13, in step (a), wherein said control circuit reads said test data in digital form from said test sample which embodies a digital circuit.

18. (Previously Presented) The method as recited in claim 14, in step (a), wherein said control circuit reads said test data in digital form from said test sample which embodies a digital circuit.

19. (Previously Presented) The method as recited in claim 16, in step (a), wherein said control circuit reads said test data in digital form from said test sample which embodies a digital circuit.

20. (Previously Presented) The method as recited in claim 17, in step (a), wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time interval.

21. (Previously Presented) The method as recited in claim 18, in step (a), wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time interval.

22. (Previously Presented) The method as recited in claim 19, in step (a), wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time interval.